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EXPLORING SLICING-BASED DESIGN TECHNIQUE FOR LOW-NOISE CHARGE-SENSITIVE AMPLIFIERS IN CMOS TECHNOLOGY

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Abstract—**The text expounds upon the contemporary condition of computer-aided design (CAD) instruments for analogue integrated circuits (ICs), alongside recent breakthroughs in this domain. The text elucidates the disparities between digital and analogue integrated circuit (IC) design, underscoring the fact that while digital design is predominantly mechanized, analogue design persists as a laborious and erudition-dependent undertaking. The excerpt expounds upon a novel methodology for designing analogue integrated circuits, which is predicated upon the utilization of slice-based techniques. The primary objective of this approach is to mitigate the temporal and cognitive demands imposed on the user. The employed methodology entails the utilization of preconceived circuit cells that can be interconnected in parallel to effectively amplify crucial performance metrics. The excerpt highlights the fact that mixed-signal integrated circuits are typically composed of a minute proportion of analogue blocks. However, there is an escalating demand for computer-aided design tools that augment the efficiency of analogue IC design and enhance its quality. This is primarily due to the rising levels of integration achievable in silicon technology and the mounting necessity for digital systems to interact with the analogue external environment. The text expounds upon a multitude of design quandaries that are inherent to analogue integrated circuit design. These quandaries encompass simulation and modelling, symbolic analysis, synthesis and optimization, layout generation, yield analysis and design cantering, and testing. The text elucidates advancements in the realm of modelling methodologies for intricate integrated systems, optimization tools for analogue and RF circuits pertaining to circuit and yield, and signal integrity analysis techniques inclusive of EMC and EMI analysis. The excerpt posits an alternative approach to instructing individuals in the realm of analogue integrated circuit design. It asserts that solely undertaking analyses that are geared towards design is the only worthwhile pursuit and that the outcomes should be conveyed in expressions that exhibit low entropy. The text comprises an uncomplicated analogue circuit instance that serves as an exemplar of a technique for design-oriented analysis. Performing algebraic operations on the circuit diagram the passage elucidates that in high-energy physics experiments, charge amplifiers are the conventional approach to amplify signals from capacitive detectors. However, the resolution attainable is restricted by the noise emanating from the input transistor of the charge amplifier. The excerpt presents a novel methodology for noise analysis in charge amplifiers, which involves an extension of the existing approach that amalgamates circuit equations and outcomes derived from SPICE simulations.**

Keywords: **Charge-sensitive amplifiers (CSA), low-noise amplifiers, noise, slice-based design, and electronic design automation (EDA).**

I. INTRODUCTION

Smaller process technologies and more complex integrated circuit (IC) designs have resulted from the advancement of consumer electronics. Digital IC design has advanced thanks to Electronic Design Automation (EDA) tools, but analogue IC design is still largely done by hand by designers [1]. The analogue design process is a difficult, knowledge-intensive task with many different performance requirements that are frequently in conflict. A custom optimized design that has a

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thorough understanding of device behaviour and design trade-offs is necessary for the circuit-level design. A solution utilizing regulated-cascode stages is suggested to address the design difficulties of gain-boosted CMOS operational amplifiers. The gain-boosted op amp's transition frequency may experience a pole-zero doublet, which would impair the transient response and negate the usual stability-based design criterion. In order to get around the limitations of intuitive analysis, symbolic analysis techniques are used to optimize the step function response of the gain-boosted op amp. The study shows that it is also necessary to consider the behaviour of a pair of complex conjugate poles, and a new design criterion is suggested for optimizing the settling time as opposed to the phase margin. It is suggested to use a synthesis method based on the "gm/ID" methodology for actual design cases [5].

A. The Significance of Systematization and Automation

In order to enhance the efficacy of analogue integrated circuit design, designers employ Computer-Aided Design (CAD) tools such as circuit simulators, layout editors, and verification tools. The existing disparity in productivity between analogue and digital circuits can be attributed to the nascent state of Electronic Design Automation (EDA) tools for analogue design, an area that remains the subject of ongoing research [6]. Analogue Design Automation (ADA) comprises a hierarchical triad of topology selection, specification translation, and layout generation. The process of topology selection involves the discernment of the most suitable circuit topology that aligns with the given requirements. The process of translating high-level specifications into lower-level sub-blocks and device sizes is accomplished through the mechanism of specification translation. Finally, it is worth noting that the process of layout generation involves the intricate arrangement of sub-blocks at a granular level, alongside their strategic placement and routing at a macro level. The subjects' historical contours have been subjected to literary analysis [9].

B. Refining Analog Circuit Performance through the gm/ID Design Methodology

Analogue designers place significant reliance on manual analysis and circuit simulation techniques at the circuit level to obtain low-entropy expressions that are appropriate for the design process. The gm/ID methodology is a technique that facilitates the systematization of this process. The approach in question employs tables that incorporate gm/ID-dependent parameters derived from meticulous simulation outcomes, in conjunction with gm/ID, a design variable that signifies the extent of inversion of a transistor. The implementation of this approach yields a heightened level of acuity in the design process [11].

The fundamental basis of the gm/ID methodology is a concept that is easily comprehensible. Let us contemplate a transistor possessing dimensions of W x L, which is subjected to a particular operating point. The parameters of interest include ID for drain current, gm for transconductance, and Cgs for gate-to-source capacitance, as documented in reference [12.

II. A METHODOLOGY FOR DESIGNING BASED ON SLICE-BY-SLICE ANALYSIS

The slice-based design methodology is an innovative approach to analogue design that leverages a repository of pre-optimized circuits, referred to as "slices," to expedite the design process. The desired performance metrics can be attained by connecting these slices, which are indivisible cells, in parallel. The number of iterations required to arrive at an optimized design is decreased using pre-characterized circuit cells, which minimize performance uncertainty. However, creating a library of fully optimized and characterized circuit slices is necessary for this methodology to be successful [16].

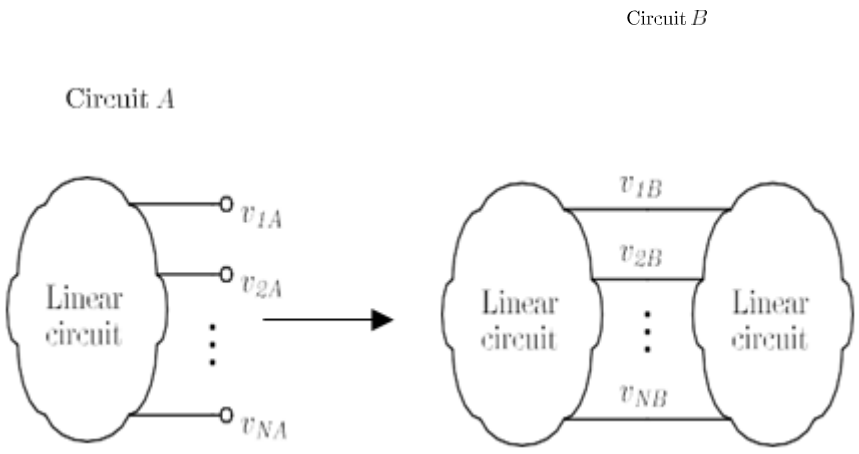

Fig. 1: Analysis and Demonstration of the Parallel Configuration of Homogeneous Circuit Replicas

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A comprehensive analysis was conducted on the utilisation of amplifiers in instrumentation for particle physics with the aim of evaluating the feasibility of this approach. The methodology can be applied to other domains, even though the analysis is particular to this application. [17].

A. Analyzing the Impacts of Parallel Circuit Interconnections on Electrical Systems

This approach is achieved by sacrificing power consumption and die area, thereby ensuring optimal performance. The concept of parallel circuitry for the purpose of augmenting drive capacity or equalizing power consumption and noise efficiency is not novel. However, the technique of linking extensive and complex circuits in parallel to amplify circuit performance has yet to be documented in scholarly publications.

1) The Standard Scenario

The Upon paralleling an exact replica of an arbitrary linear circuit, denoted as circuit A, at each of the N nodes, circuit B undergoes alterations in certain figures of merit and quantities, while retaining its original form. Specifically, the M branch currents exhibit a twofold increase whilst the N node voltages remain unaltered. These modifications happen as a result of the parallel connection's altered perception of impedance by the sources connected to the nodes.

$$v_{iB} = v_{iA} \quad (1)$$
$$i_{jB} = 2i_{jA} \quad (2)$$

The parallel connection reduces all impedance components Zk in circuit B by half while increasing all admittance components Yk, including transconductances. Due to the parallel connection's reduced effective impedance as seen by the sources, current and voltage are increased and decreased, causing this effect [20].

$$Z_{kB} = Z_{kA}/2 \quad (3)$$
$$Y_{jB} = 2Y_{kA} \quad (4)$$

Both equivalent node impedances and explicit passive components like resistors, capacitors, and inductors exhibit the effect. The branch currents double, which results in a doubling of power consumption in circuit B. However, because the gm/ID ratio is unaffected, the operating point of all MOS devices is unaffected [22].

2) First-order active low-pass filter

When multiple circuits are paralleled with the amplifier, it can be observed that the effective transconductance G_{meff} increases while the output resistance R_{Out} decreases. As per reference [25], it can be inferred that the open-loop gain remains constant. The aforementioned outcome can be elucidated by the parallel connection's capacity to augment current whilst diminishing equivalent impedance, thereby elevating effective transconductance. In another direction connections reduce the actual resistance of the load observed by the amp's output, which decreases the output opposition.

$$AB = G_{meffB} \cdot R_{OutB} = 2G_{meffA} \cdot R_{outA}/2 = A_A \quad (5)$$

Similar to this, the single-pole amplifier's bandwidth is impacted by the parallel connection of identical circuits. In the resulting circuit, the equivalent capacitance of the dominant pole is specifically doubled while the equivalent resistance experienced by the capacitor is reduced by half. This effect results from the parallel connection's ability to lower the effective impedance that the capacitor perceives, which increases current and, in turn, capacitance [24]. At the same time, the effective resistance observed by the capacitor, decreases, which causes the dominant pole frequency to decrease and, as a result, increases the amplifier's bandwidth.

Table 1: Normalized MOSFET noise equations

	$\overline{V_n^2}/\Delta f$	$\overline{\hat{V}_n^2}/\Delta f$
Thermal noise for strong inversion	$\frac{4k_BT\gamma}{g_m}$	$4k_BT\gamma\left(\frac{I_D}{g_m}\right)$
Shot noise for weak inversion	$\frac{2qI_D}{g_m^2}$	$2q\left(\frac{I_D}{g_m}\right)^2$
HSPICE 1/f noise (NLEV=0)	-	-
HSPICE 1/f noise (NLEV=2, 3)	$\frac{K_F}{C_{ox}WLf^{A_F}}$	$\frac{K_F}{C_{ox}Lf^{A_F}}\left(\frac{I_D}{W}\right)$
BSIM 3 thermal noise	$\frac{4k_BT}{g_m^2R_{DS}+L^2g_m^2/(\mu\lvert Q_{inv}\rvert)}$	$\frac{4k_BT}{g_mR_{DS}+L^2g_m/(\mu\lvert Q_{inv}\rvert)}\left(\frac{I_D}{g_m}\right)$
BSIM3 1/f noise for strong inversion	$\frac{k_BT}{L^2f^{E_F}}\left(\frac{q^2\mu I_DW_A}{g_m^2C_{ox}}+\frac{I_D^2\Delta L_{clm}W_B}{g_m^2qW}\right)$	$\frac{k_BT}{L^2f^{E_F}}\left(\frac{q^2\mu W_A}{C_{ox}}+\frac{\Delta L_{clm}W_B}{q}\left(\frac{I_D}{W}\right)\right)\left(\frac{I_D}{g_m}\right)^2$

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$\omega_{cB} = 1 / R_{eqB} \cdot C_{eqB} = 1 / (R_{eqA}/2 \cdot 2C_{eqA}) = \omega_{cA}$ (6)

It is important to note that in real-world circuits, the external load frequently determines the bandwidth. Thus, if the external load is also connected in parallel, the bandwidth is unaffected. The bandwidth, however, might change as a result of the parallel connection if the external load is not parallel-connected. The parallel-connected amplifier, however, has twice the drive capacity of the single circuit, which may be advantageous in some applications [16].

3) Characterizing and Quantifying Noise in Signal Processing Systems: An Analysis

In Let us contemplate a linear circuit that encompasses a solitary noise generator, for instance, a resistor that engenders thermal noise. It can be observed that the power spectral density (PSD) of the noise exhibits a direct proportionality with respect to its resistance when expressed in voltage variance, while an inverse proportionality is observed when expressed in current variance. Upon connecting two identical circuits in parallel, it can be observed that the equivalent resistance values undergo a halving process. This leads to a reduction in the voltage noise power by half, while the current noise power is doubled. As the voltage signals remain unaltered, the ratio of the squared voltage signals, also known as the signal-to-noise ratio (SNR), experiences a twofold increase.

$$\frac{\overline{V_n^2}}{\Delta f}(f) = 4kTR\left[\frac{v^2}{Hz}\right], \frac{I_n^2}{\Delta f}(f) = \frac{4kT}{R}\left[\frac{A^2}{Hz}\right] \quad (9)$$

The noise emanating from thermal, shot, and flicker sources in a solitary MOSFET transistor can be standardized and articulated as a gm/ID ratio-dependent function.Upon connecting two identical circuits in parallel, it can be observed that the equivalent transistor drains current experiences a twofold increase, while the gm/ID value remains constant. The outcome of this phenomenon is a reduction in the variance of voltage noise by half and an amplification of the variance of current noise by two-fold. Consequently, the signal-to-noise ratio (SNR) is enhanced by a factor of two for both voltage and current noise[18].

In the context of a linear circuit featuring multiple noise generators, one may derive the aggregate noise present at the output node by utilizing the Power Spectral Density (PSD) of each distinct noisy device in conjunction with the transfer function that corresponds to each individual noise source's contribution to the output. This process may be facilitated by consulting Table 1 for relevant data. Due to the independence of the noise generators, their respective noise contributions are uncorrelated and are combined through the process of quadrature addition.

B. A Systematic Design: Principles and Processes.

1) The Pre-Design Stage in Technical Terms

The task of an analogue designer entails the creation of distinct segments within the conventional analogue design workflow. Each segment is meticulously tailored to fulfil a particular set of requirements, encompassing various aspects of the design domain, such as the highest attainable gain-bandwidth product or the lowest possible noise, as exemplified by amplifiers [6].

These equations are integral components of the slice documentation. As per the reference [8], it is plausible to recalculate and compile the equations for higher branch currents upon the parallel connection of the slices. It is noteworthy that the increments of the currents solely occur in whole numbers of the unit slice, which represents an indivisible entity.

At the level of layout design, it is imperative to ensure that each slice is optimized for parallel connectivity with numerous layout blocks. A plausible strategy would be to execute every segment in a rectangular configuration, whereby the inputs and outputs are situated on the periphery and all interconnecting nodes are aligned parallel to the y-axis. It is possible to allocate one or more metallic strata for the purpose of internal nodal tracings to enable parallel connections, while the other strata are dedicated to achieving a more condensed design.

It should be noted that the determination of the most suitable geometry with regards to factors such as intra-cell device matching or minimum die area is beyond the purview of this document and necessitates additional analysis. The bias circuitry associated with each slice may be either integrated within the slice or fashioned as a distinct, autonomous slice. It is feasible to effectuate an optimized outcome for a given application by customizing the layout, albeit necessitating an individualized design, even if a specific slice is subject to arbitrary scaling at the circuit level [13].

2) STAGE DESIGNING OF SLICE

The implementation of the slice-based design methodology necessitates the development of a repository of finely-tuned and exhaustively characterised slices, encompassing transistor-level schematics, physical layouts, and accompanying documentation. Each slice has been meticulously optimised to cover distinct corners of the design space, such as the maximal gain-bandwidth product or the minimal noise. The operational state of every device within the slice is determined by its respective current and gm/ID. It is feasible to calculate the slice's small-signal behaviour based on the distinct device parameters, and these formulae are included in the slice records [16].

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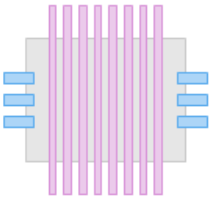
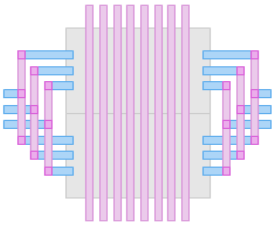


(a) Single slice



(b) Two slices in parallel
Fig2.suggested layout and parallel-connection plan [1]

In order to implement the slice-based approach, the integrated circuit designer must exercise discretion in selecting a pre-existing slice from the library and subsequently scaling it by interconnecting multiple copies in parallel. After the design phase, the validation of the circuit is carried out via SPICE simulations. In the event of any discrepancies, the biassing circuit can be fine-tuned to regulate all currents. Upon completion of the circuit, a thorough evaluation of its adherence to the desired specifications is conducted. The layout is then meticulously crafted by arranging the slices in a predetermined scheme that involves stacking and abutting. The automation of the layout task may be facilitated by employing Electronic Design Automation (EDA) tools, as referenced in [13].

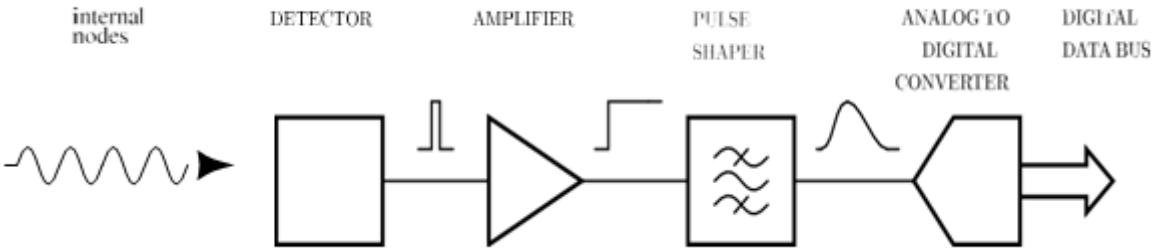


Fig 3: A schematic representation of a singular channel within a universal pulse processing circuit utilized in experiments pertaining to the field of particle physics [1]

The utilization of a repository containing preconceived and thoroughly evaluated circuit fragments serves to curtail the duration and ambiguities that are typically associated with analogue design components, ultimately yielding a streamlined design methodology. It is feasible to effectuate an optimized outcome for a specific application through a personalized layout, albeit necessitating a bespoke arrangement, by subjecting a given slice to arbitrary scaling at the circuit level.

C. ADJUSTABLE PERFORMANCE OF SLICING

Theutilization of the slice-based design methodology confers the benefit of enabling the creation of circuits that possess the ability to adaptively adjust their scale to fulfil performance demands. The objective is accomplished through the utilization of switch banks for the purpose of interconnecting and energizing diverse quantities of parallel-connected circuit slices. This approach enables the adjustment of the quantity of active circuit duplicates in accordance with dynamic specifications, while simultaneously minimizing power consumption, as documented in reference [3].

D. POTENTIAL ISSUE TECHNIQUE

The employment of the slice-based design methodology proffers a plethora of benefits; nevertheless, it is imperative to consider certain cautionary considerations during the execution of the arrangement. The utilization of traces to connect slices in a parallel configuration entails the presence of intrinsic parasitic elements that may exert an impact on the overall performance. The impact of said parasitic components is contingent upon the specific circuit under consideration. Subsequently, as the quantity of parallel-connected slices rises, the spatial separation between said slices may attain a magnitude that gives rise to inconsistencies pertaining to process gradients. The ramifications of this phenomenon can be quite substantial with regards to the overall efficacy of the circuit. Tertiary, incongruities may also yield dissimilarities in voltage amidst ostensibly indistinguishable nodal points, thereby engendering electric current transmittance across the interconnecting wires of the parallelly linked segments [13].
The occurrence of this phenomenon can be attributed to discrepancies in both gradient and size. It is of utmost

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importance to comprehensively comprehend and scrutinize each of these caveats, as they possess the potential to exert a substantial influence on the performance of the circuit. The current manuscript solely examines the impact of gradient-induced incongruity, as it appears to be pertinent to the acquired measurement outcomes. Depending on the technological framework, circuit topology, and intended use, alternative concerns may emerge as preeminent, such as the presence of wire parasitic. Hence, it is imperative to contemplate every conceivable source of fallacy and devise considerations when executing the slice-based design methodology.

III. TOPIC AT HAND PERTAINS TO THE PRESENCE OF EXTRANEOUS SIGNALS IN THE REALM OF PARTICLE PHY

The creation of circuitry for particle phy expts is a multifaceted and intricate endeavour that involves a plethora of factors and variables spanning the domains of system, circuit, and layout. Given the idiosyncratic demands of each distinct challenge, a bespoke resolution is requisite. Moreover, it is noteworthy that even a minor modification in the parameters of an application can result in a circuit that was previously engineered to be suboptimal, either by failing to satisfy the necessary specifications or by consuming an excessive amount of power [19]. Hence, the prospect of employing pre-existing designs for novel predicaments is not a feasible alternative, thereby rendering particle physics instrumentation as a prime contender for evaluating the suggested design methodology. This segment offers a succinct synopsis of the relevant principles pertaining to instrumentation in the field of particle physics, as well as the analysis of noise.

A. EXPERIMENTS OF ELECTRONICS AND PARTCLE PHYSICS

The diverse array of particle physics detector systems is accompanied by a range of electronic components that carry out essential operations. To conduct further analysis, it is necessary to procure, enhance, refine, and retain the signals obtained from the detector channels. The channel responsible for detection comprises a sequence of components, namely a detector, amplifier, filter, ADC, and r_d out circuit, as expounded in reference [4]. The third figure presented herein proffers a streamlined schematic representation that elucidates the constituent elements of a standard detector channel within a universal particle physics detector system.

B. FRONT-END OF THE ANALOG

Within the context of a particle physics detector system, it is observed that the detector possesses the ability to transform the energy of an incoming particle into an electrical charge denoted as Q_in. The magnitude of this electric charge is directly proportional to the quantity of energy that has been assimilated by the detector. The initial stage of signal amplification involves the conversion of charge into a voltage signal via the transfer of charge from the detector's nonlinear capacitance, C_D, to a capacitor of known value, C_F, by means of the front-end amplifier. The expression for the output voltage V_out of the amplifier can be represented as V_out = Q_in/C_F, where Q_in denotes the input charge and C_F represents the capacitance of the feedback network. The gain of the amplifier is commonly quantified in units of [V/C] or [F^-1] [19]. The preeminent preamplifier implementation utilised in instrumentation for particle physics is the charge-sensitive amplifier (CSA). This consists of a voltage amplifier with a capacitor in negative feedback configuration. Subsequent to the generation of the CSA's output, it is subjected to a filter that enhances the signal-to-noise ratio (SNR) by implementing a band pass filter that suppresses noise whilst amplifying the signal. The filter possesses the ability to modify the temporal characteristics of the input signal and is commonly denoted as a pulse shaper in literature [7].The transfer function H(jω) is utilised to model the pulse-shaping filter. The circuit includes a reset element, represented by resistor R_rst, which discharges the feedback capacitor. The element utilised for resetting purposes may take the form of a gate-controlled switch or a resistor, serving to facilitate instantaneous or continuous-time discharge, correspondingly.

C. EQUIVALENT NOISE CHARGE(ENC)

For assessing a front-end circuit's noise properties in particle physics instrumentation, the Equivalent Noise Charge (ENC) metric is frequently used. The quantification of the ENC is determined through the counting of electrons, and is defined as the minimal i/p charge necessary to produce an output SNR of 1. It can be represented mathematically as:

$$\mathrm{ENC} = \sqrt{\frac{\overline{v_{0,N}^2}}{v_{0,e}^2}} \qquad [9]$$

Where vo,e is the peak amplitude of a single input charge electron in the absence of noise, determined by vo,e = q CF maxg(t), and V2O,N is the total integrated output-referred noise of the analogue front-end. A lower ENC value indicates better noise performance, making it easy to compare the noise performance of various front-end circuits [15].

$$V_{0,e} = \frac{q}{c_f}\max\{g(t)\} \qquad [10]$$

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IV. THE IMPLEMENTATION OF A CONFIGURABLE CSA DESIGN SERVES AS THE FOUNDATION FOR A PRACTICAL APPLICATION

To assess the practical implementation and effectiveness of a front-end circuit constructed using the proposed approach, a customised integrated circuit and printed circuit board (PCB) were utilised to realise a front-end circuit for experiments in particle physics. The development of an integrated circuit was undertaken, utilising a 0.5-µm CMOS technology. The circuit was designed to incorporate a configurable charge-sensitive amplifier (CSA) for the purpose of analysing the scaling behaviour of the output noise. This was achieved through a gradual increase in the number of amplifier slices connected in parallel, as detailed in references [9]-[11].

A. DESIGNNING OF SYSTEM-LEVEL

The block diagram depicted in the testing system is primarily composed of a pulse processing chain, commonly utilized for noise performance evaluation of integrated circuits. The naming convention used in this document is based on the hierarchical order of the IC, test board, and test system. During testing, a detector was not used, and instead, an explicit large capacitance CD was emulated on the test board along with a pre-charger circuit that injects a precise amount of electrical charge [13]. The magnitude of electrical charge that is deposited by the pre-charger is precisely controlled by a 12-bit digital-to-analog converter, which is conveniently located on the test board. The visual representation in Figure 7 portrays the circuit block diagram of the chip, which has been partitioned into four discrete functional blocks. These blocks include the pre-chrg ckt, the configurable amp, the feedback n/w, and the o/p buffer.

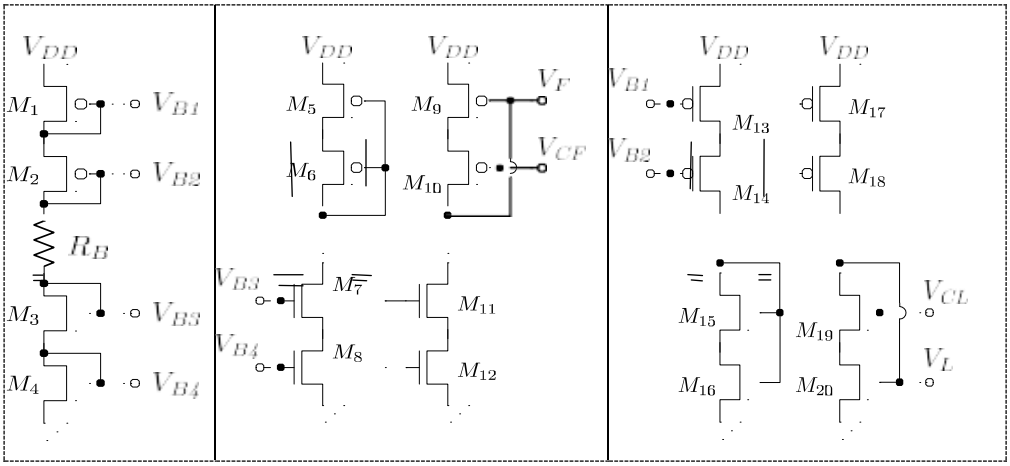

Fig4.Systemblockdiagram of testing [1]

The configurable amplifier is a composite of 8 identical amp's slices that can be interconnected in parallel switched, employing a thermometer mode for the connection process. The current mode enables the sequential interconnection of amplifier slices, whereby the sequence adheres to the pattern of $\{1\}, \{1-2\}, \{1-2-3\}, \ldots, \{1-2-\ldots-8\}$.

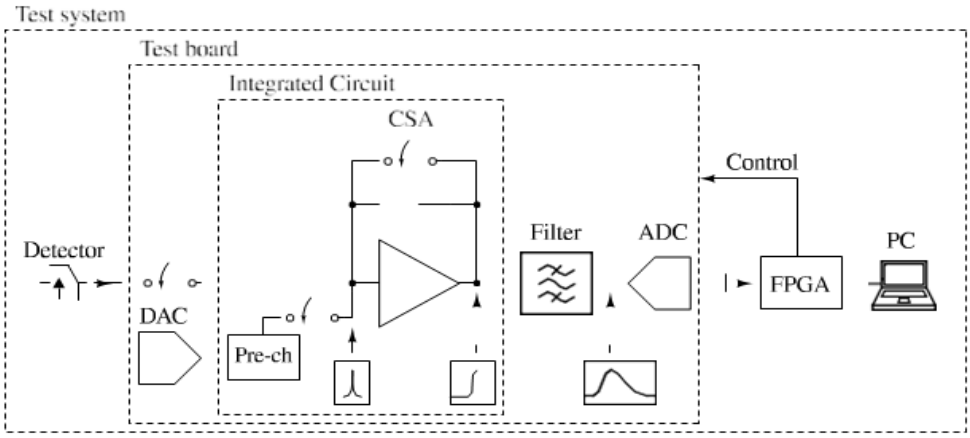

Fig 5: Schematic Diag. for the amplifier bias circuit [1]

International Journal of Engineering Applied Sciences and Technology, 2024
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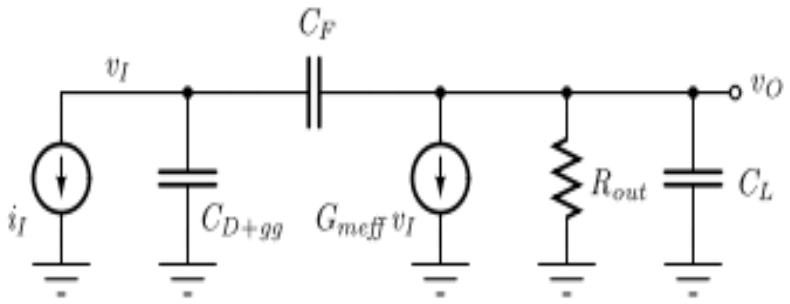
Accordance with the numerical labelling of the amplifier segments depicted in Figure 7.The impact of load capacitances on the CSA's sensitivity can potentially constrain the amplifier's bandwidth, trigger instability, and ultimately result in output slewing. To address this particular concern, a v/t buffer was strategically incorporated along the s/n pathway to prevent any unwarranted loading on the CSA o/p, as documented in reference [12].

A. CkT DESIGNING TOPOLOGY

The folded-cascode topology was employed in the design of the CSA, utilizing an N-channel MOSFET input device. Each amplifier slice consisted of eight identical amplifier units connected in parallel via switches. The gain was found to be independent of the number of amplifier slices connected in parallel, due to the proportionality between Gmeff and Rout. The frequency response of the amplifier was dominated by a single pole, defined by the output resistance and a load capacitance [17]. The bias circuit was included in each amplifier slice, with separate bias voltages generated for each transistor. The circuit was designed to minimize loading effects on the CSA output, with a voltage buffer added to prevent excessive loading.



. Fig 6: The schematic depicting s/s behaviour of the closed-loop current sense amplifieris utilized for the purpose of analyzing frequency response

1) Parameters of interest in a current sense amplifier

The calculation of the low-frequency, open-loop gain of the folded-cascode amplifier is predicated on the multiplication of the effective t/cG_{meff} and the o/p resistance. Through the application of circuit analysis methodologies and under the condition of high intrinsic gain ($g_m r_o$) exhibited by the transistors, one can derive estimations for the values of G_{meff} and Rout:

$G_{meff} \approx g_m I$ and [16]
Rout ≈ ($g_m C_L r_o C_L roL$) k ($g_m C_F r_o C_F$ ($r_o I$ k $r_o F$)) [17]

If two amps slices are interconnected in parallelly, the G of the resultant amp is commensurate to that of a solitary slice, on the condition that Gmeff escalates proportionally to the abatement in Rout [8].

2) FREQUENCY REUSE OF CSA

Based on Figure 11, it can be deduced that the closed-loop bandwidth of a Constant Fraction Discriminator (CFD) does not remain fixed when multiple slices are connected in parallel. This is attributed to the fact that the effective transconductance Gmeff changes with an increase in the number of slices, causing a change in the closed-loop bandwidth.

$$\frac{V_O(s)}{I_I(s)} = \frac{1}{sC_F} \cdot \gamma_{ol} \cdot \left[\frac{1 - s/z}{1 - s/p}\right] \quad [18]$$

Where,

$$\gamma_{ol} = \frac{G_{meff} R_{out} \cdot C_F}{(1 + G_{meff} R_{out}) \cdot C_F + C_{D+gg}} \quad [19]$$

However, the exact proportional relationship between the number of slices and the increase in closed-loop bandwidth is not immediately apparent since the external capacitances that determine the bandwidth, such as CD, CL, and CF, remain unchanged [19].

$\mathbf{z} = \frac{\mathbf{G_{meff}}}{\mathbf{C_f}}$,

$$p \approx -\frac{G_{meff} \cdot C_F}{C_L \cdot C_F + C_L \cdot C_{D+gg} + C_F \cdot C_{D+gg}} \quad [22]$$

Despite this, the overall speed of the circuit is ultimately governed by the peaking time of the pulse-shaping filter, which should be significantly shorter than the CSA time constant to prevent a slowdown in the circuit's nominal speed.

International Journal of Engineering Applied Sciences and Technology, 2024
Vol. 8, Issue 11, ISSN No. 2455-2143, Pages 98-113
Published Online March 2024 in IJEAST (http://www.ijeast.com)

3) NOISE OF INPUT-REFFERED

The input-referred noise of the folded-cascode amplifier can be calculated by summing the input-referred noise contributions of each individual transistor, which are determined by their gate-referred noise power and low-frequency, open-loop transfer fxn to the input of the amp. The t/ffxn of each transistor is primarily influenced by external factors.

$$\mathbf{V_{I,N}^2(jw) = \sum V_{n,i}^2(jw) \cdot H_i^2} \qquad \textbf{[23]}$$

In the context of the NMOS-input folded-cascode amplifier, one may derive the transfer fxn of each transistor and subsequently deduce that the parallel connection of two amplifier slices would not exert any influence upon the transfer fxn of each individual transistor. As per the findings of reference [22], it can be inferred that the gate-referred power spectral density of individual transistors would undergo a 50% reduction, thereby leading to a commensurate reduction in the aggregate input-referred noise.

The introduction of noise by the amplifier's bias circuitry can be ameliorated through the incorporation of substantial bypass capacitors on the nodes responsible for DC bias. The incorporation of the bias circuit in each slice of the designed integrated circuit has a discernible effect on the overall noise output, while simultaneously preserving the accuracy and soundness of the outcomes.

4) CSA PARALLELY CONNECT

Figure 11 shows the IC's connected parallelly to the plan for the amplifier slices. The switch bank, consisting of CMOS switches, connects all internal nodes of the amplifier between adjacent slices, except for the input and output nodes. A single control signal, swn, is used to control the switches [27]. To guarantee that all slices are exposed to the same signal path, the i/p and o/p nodes of each slice are additionally connected using CMOS switches to a common wire. The series resistance of the CMOS switches is minimal. A micrograph of the reconfigurable CSA on the IC is shown in Figure 12

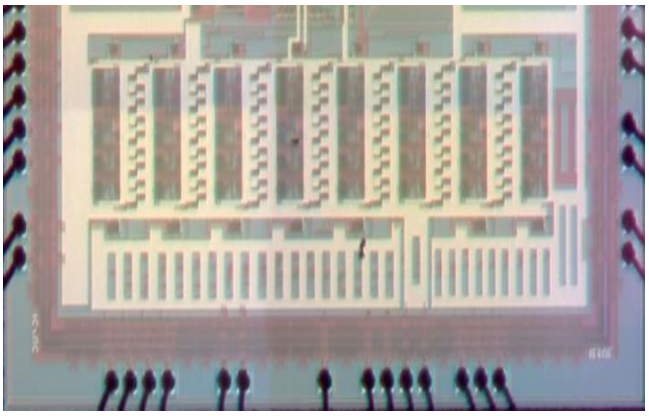


Fig 7:Micrograph view configurable CSA on the IC [1]

5) PULSE SHAPING FILTER

The utilisation of a printed circuit board for testing purposes has facilitated the implementation of a pulse-shaping filter that employs a linear time-invariant CR-2RC topology, utilising discrete components. The filter underwent an assessment of its peaking time, designated as P and quantified over a duration of 20 seconds. In order to attain the maximum value of unity peak for the unit step response of the filter, denoted as g(t), a pair of gain stages were integrated to offset the reduction in amplitude caused by the filter.

6) SCALING OF BANDWIDTH AND NOISE PSD

While the capacitances that determine bandwidth largely remain unchanged, connecting 2 CSA slices in parallel raises the circuit's effective transcondt^{n} and widens its b/w. However, in this scenario, each transistor's contribution to the voltage noise spectral density is cut in half. Since the PSD of the noise would decrease while the circuit's bandwidth would increase, measuring the noise directly at the CSA output would not clearly improve the total integrated noise performance [21]. However, a definite reduction in CSA noise can be seen when additional slices are connected in parallel by monitoring the noise at the output of the cascade-connected pulse-shaping filter, which restricts the circuit's bandwidth.

B. IMPLEMENTATION OF CSA

The configurable CSA is implemented on the integrated ckt in the partial chip micrograph shown in Figure 12.

1) FLOORPLAN MODELING

Figure 13's partial chip floor plan shows the layout of the integrated circuit, with the configurable amplifier's amplifier slices and switch banks shown on the left side of the picture. The pre-charger circuit, feedback network, and output buffer are visible in the right corner of the image [12].

2) SLICE AND PARALLEL CONNECTION OF AN AMPLIFIER

The folded-cascode amplifier and the bias circuit are integrated into the layout of a single amplifier slice, as shown in Figure 14, to locally match both the amplifier and the bias devices. The slice's dimensions are 421.5 m 177.3 m, and it has voltage rails that are clearly separated on either side that were designed after digital cell layouts. The internal node traces and the slice's inputs and outputs both follow the x-axis in a parallel fashion in line with the y-axis.

International Journal of Engineering Applied Sciences and Technology, 2024
Vol. 8, Issue 11, ISSN No. 2455-2143, Pages 98-113
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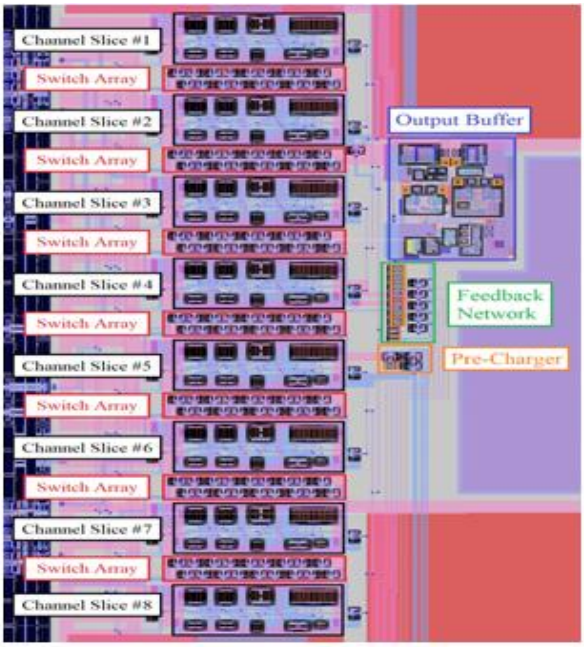

Fig 8.For the NMOS-input CSA channel, the chip floor plan [1]

The chip was not designed using this method, which would have allowed testing of various numbers of parallel-connected slices. Each node in the switch bank has a corresponding CMOS switch, allowing for the connection and disconnection of neighboring slices as well as adjusting the performance of the equivalent circuit. The switch bank's addition raises the cell pitch to 276.6 m.

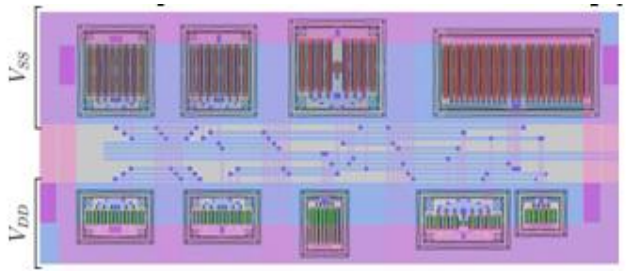

Fig 9: The arrangement of amplifier slices in fold-cascode [1]

V. REFERRING TO EXPERIMENTAL FINDINGS OR RESULTS

Two different types of measurements were made to gauge the configurable CSA's performance:

A) CSA STEP REACTION

Two different types of measurements were used to test the configurable CSA: avg w/f measurements to assess its overall fxnlty and statistical o/p voltage measurements to assess noise performance. The step response of the CSA for various values of k is shown in Figure 16(a).

1. STEP AMPLITUDE OF CASCODE

Using an oscilloscope to measure the voltage buffer's output and avgng 8,192 identical events to reduce noise, the step response was examined. Equations (29) and (30) predict the step amplitude for an injected chrg Qin, where ol(k) is the static attn^{n} of the amp.

$$\mathbf{v_0(k) = \gamma_{0l}(k) \cdot \frac{Q_{in}}{c_f}}$$

Due to a parasitic feedback capacitance component that scales with k, the step amplitude slightly decreases as k increases [18]. However, the step amplitude's behaviour is consistent with simulations and hand calculations' predictions.

2. BANDWIDTH CASCODE MODEL

The interplay between a folded cascode amplifier (CSA) operating in current mode and a bandpass pulse-shaping filter is known to have a notable effect on the amplifier's bandwidth, as the filter serves to reduce noise. The significance of the amplifier's bandwidth is negligible providedthat the amplifier exhibits a substantially higher speed than the filter.

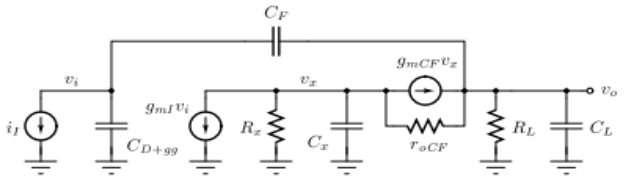

Fig 10: Schematic of S/s Analysis of NMOS-I/p Folded-Cascode Amp with Capacitive Feedback and Non-Dominant Pole Compensation[1]

The single-pole approximation can be used to specify and express explicitly the expected bandwidth for the CSA as a function of the scaling factor, k. The i/p capacitance of the buffer and the output capacitance of the CSA together make up the load capacitance, CL(k), which scales with k. Due to the predominance of non-scaling capacitances, the bandwidth increased when two amps slices are connected in parallel is only capable of increasing by a factor of two at most [1]. Under any other circumstance, however, the capacitance values determine how the bandwidth scales in a manner that is not immediately apparent.

$$\mathbf{C_l(k) = k.C_{lcsa} + C_{Lbuf}} \qquad [1]$$

The slight overshoot in the step response for some of the curves shows that the output of the CSA behaves in practice like a second-order circuit.The circuit transitions from being overdamped to being underdamped as the scaling factor increases, indicating that the behaviour of the amplifier's bandwidth is consistent with expectations, according to a numerical evaluation of the damping factor using the corresponding amplifier parameters [4].

International Journal of Engineering Applied Sciences and Technology, 2024
Vol. 8, Issue 11, ISSN No. 2455-2143, Pages 98-113
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B) Overview of Noise Measurement Techniques and Considerations

The present inquiry involved an empirical investigation of the acoustic attributes of a modifiable current sense amplifier (CSA) across a range of k values (1-8) and CF values (1-8 pF, with increments of 1 pF). The output of the CSA was linked to a CR-2RC filter, and subsequently, the resultant noise signal underwent sampling and quantification via a 16-bitADC. The computation and recording of the variance of 75k voltage samples were executed for every k and CF combination, as documented in reference [15].

Figure 11 displays the data that has been gathered and plotted on a semi-logarithmic scale. Each point on the graph corresponds to the variance of the noise signal. The noise signal's scaling behaviour as a function of k and CF was illustrated by generating curves through connecting the data points with straight lines.

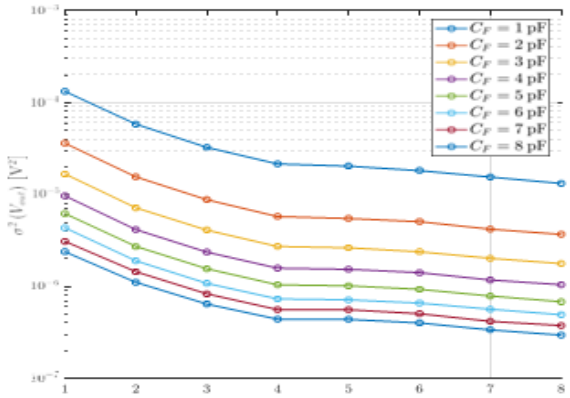

Fig 11:Noise measurements for all CF and k combinations

1. Total Integrated Noise in Electronic Circuits: An Understanding

Since the configurable CSA lacked a detector, we could ignore its noise contribution to the equivalent noise charge (ENC) equation when measuring the noise characteristics of the system.As a result, the pulse-shaping filter's output's total integrated noise was roughly represented as a voltage variance that only depends on amplifier contributions. A function of k, the number of parallel-connected CSA slices, and different amplifier parameters can be used to express this noise [23].Subsequently, the noise terms were employed to deduce a lucid formulation for the aggregate integrated noise. This formulation evinced an inverse correlation with the quantity of CSA slices that were connected in parallel [23]. Moreover, the test board was equipped with a substantial explicit capacitor CD, surpassing the cumulative gate capacitance C_{gg} of the adaptable CSA. The present configuration has yielded a noise mitigation outcome that is inversely proportional to the quantity of CSA slices that are connected in parallel. A comprehensive evaluation was conducted on the input-referred white and flicker noise of transistors MI and MF. This analysis yielded valuable observations regarding the determinants that influence the noise properties of the CSA.

2. Investigating Non-Normal Noise Variance Distribution's Effect on Mismatch Scaling

This study delved into the noise scaling characteristics of a charge-sensitive amplifier (CSA) via an examination of its integrated noise curves relative to the quantity of parallel-connected slices. The empirical findings suggest that the noise scaling proclivities, in relation to k, remained largely unaffected by the feedback capacitance CF. The latter emerged as an autonomous variable with a tenuous correlation to k. Henceforth, it is plausible to employ any of the curves for scrutinizing the scaling of the noise. The observed aberration of the curves from the anticipated pattern ($\propto 1/k$) may be ascribed to incongruity in device dimensions and gradients [14].

In order to validate this conjecture, a Monte Carlo simulation was executed utilizing credible values for the mismatch variances. Subsequently, the integrated noise curves were graphed for all 2000 iterations. Usually, the incongruity exhibited minimal influence on the conduct of the commotion and the magnitude of the calibration. Nevertheless, in certain exceptional instances, there were conspicuous aberrations from the anticipated noise scaling. Two instances were proffered, chosen with particularity due to their resemblance to the recorded graphs.

It is imperative to acknowledge that the elucidation is not definitive, but rather a plausible explication predicated on the extant data [26]. In order to validate this hypothesis, a greater quantity of chips produced across diverse wafers would be requisite to effectively randomize and decouple the process gradients. Regrettably, the quantity of chips available for experimentation was quite limited, presumably originating from a common wafer.

VI. MISMATCH ANALYSIS FOR RESULTS INTERPRETATION

The term "mismatch" pertains to the discernible deviations in the operational output of the constituent devices within an integrated circuit, which can be ascribed to the inherent disparities in the fabrication process. The aforementioned variations can be classified into two distinct categories: systematic variations that arise from parameter gradients along the die surface, contingent upon the distance between devices, and random variations that are contingent upon device size. During the design phase, it is possible to mitigate the impact of parameter gradients through the implementation of appropriate layout techniques, such as the matching of critical transistors. The slice-based design methodology is vulnerable to gradient-induced inconsistencies owing to the utilization of pre-existing cells, which renders the implementation of layout techniques between crucial transistors on distinct slices unfeasible. Furthermore, in instances where multiple slices are

International Journal of Engineering Applied Sciences and Technology, 2024
Vol. 8, Issue 11, ISSN No. 2455-2143, Pages 98-113
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linked in parallel, transistors that are ostensibly identical may be isolated by considerable distances, thereby intensifying the consequences of disparity. Within this section, we shall undertake an analysis of the impact that alterations to parameters may have on the overall performance of circuits that have been constructed through the utilization of the design technique that has been proposed. We introduce a straightforward framework for the scaling of mismatch parameters in the context of multiple parallel-connected slices. To evaluate the soundness of our model, we conduct Monte Carlo simulations, as documented in reference [17].

A) The Mismatch Model for Improving Statistical Variability in MOSFETs

To calculate the normalizedstd[d] deviation of a p/m P between 2 MOS trnstrs on the same die separated by a distance D, Pelgrom et al. proposed the mismatch model. Equation gives the model (22),

$$\sigma^2\left(\frac{\Delta_P}{P}\right) = \frac{A_p^2}{w_L} + s_P^2 D^2 \qquad [22]$$

The comprises of a term that is dependent on the size of the transistor, which is directly proportional to its area, and another term that is dependent on the distance between the two transistors, which is directly proportional to their spacing. The chip manufacturers furnish the values of the area proportionality constant and spacing proportionality constant tailored to specific parameters. The utilization of Monte Carlo simulations is frequently employed to evaluate circuit performance due to the stochastic of m/m. The present simulations entail the addition of a random variable that conforms to a normal distribution to every parameter of each transistor within the simulated ckt netlist. This random variable is then scaled by the std[d]deviation and device size. In incorporation of the distance-dependent component in Equation (22) poses a greater challenge in its assimilation into a ckt simulator.

B) MOSFET Mismatch Model Proposed by Pelgrom

The utilization of Pelgrom's mismatch model is instrumental in characterizing the statistical fluctuations in the electrical properties of MOSFETs that arise from variances in the manufacturing process. Within the confines of this model, a particular term of note is the distance term. This term serves to denote the spatial separation between two MOSFETs that coexist on a singular microchip. The distance parameter holds a significant physical connotation as it pertains to the potential spatial inconsistencies in doping concentration and other physical attributes of the semiconductor material that may arise during the manufacturing process [18]. Consequently, the proximity of two MOSFETs during fabrication may engender slight discrepancies in their electrical characteristics owing to the heterogeneity of the semiconductor material in their vicinity. Pelgrom's model incorporates the notion that the amplitude of these fluctuations diminishes with increasing separation between the MOSFETs, as denoted by the distance parameter. The underlying reason for this phenomenon is that the semiconductor material's spatial fluctuations are generally negligible in comparison to the inter-MOSFET separation. Consequently, it can be inferred that MOSFETs situated at a considerable distance from each other are anticipated to possess analogous electrical characteristics. Conversely, MOSFETs in proximity are prone to manifest incongruity, as per references [1]-[3].

C) Understanding Mismatch Parameters in Semiconductor Device Statistical Modeling

Critical parameters can be divided into electrical and process types to efficiently model parameter mismatch. Process parameters, such as carrier mobility, are physically independent parameters that regulate a device's electrical behaviour. Electrical parameters, on the other hand, like transistor transconductance gm, are of interest to designers and are prone to deviate from their nominal values due to mismatch.

An electrical parameter's variance (e(p)) depends on n separate process parameters (p = p1, p2..., pn).

$$\boldsymbol{\sigma^2(e) = \sum_{i=1}^{n} \left(\frac{\partial e}{\partial P_i}\right)^2 \sigma^2(P_i)} \qquad [25]$$

The prevailing parameters of transistor mismatch are commonly Vt0 and β, while supplementary or alternative mismatch parameters are employed in more sophisticated mismatch models [5].

The present analysis aims not to achieve flawless precision in mismatch modelling, but to acquire a deeper understanding of the effects of device mismatch on circuit performance in the context of the suggested design methodology. Henceforth, in order to accord precedence to parsimony, this investigation shall solely consider the incongruous parameters β and Vt0.

D) Slice-Based Design Mismatch Model Refinement for Semiconductor Manufacturing

1. Parameter Scaling in Semiconductor Devices: Analysis and Modeling

Let us contemplate a circuit configuration that comprises a planar arrangement of k analogue cells, organized in a bidimensional array that extends both horizontally and vertically, with D_{cc} separating each cell. Consider M1 as a transistor arbitrarily selected from the first cell, and let $M_j$denote the corresponding transistors present in the remaining cells. Consider the parameter P as an arbitrary variable that is susceptible to discrepancies among transistors that are nominally identical. The determination of parameter P pertaining to transistor M_j can be mathematically represented as the summation of a standard value, a methodical deviation for the semiconductor dies, and two incongruent constituents,

International Journal of Engineering Applied Sciences and Technology, 2024
Vol. 8, Issue 11, ISSN No. 2455-2143, Pages 98-113
Published Online March 2024 in IJEAST (http://www.ijeast.com)

signifying distance-oriented and stochastic fluctuations. The term that varies based on the distance between transistors can be expressed as the result of multiplying a plane gradient by said distance.

$$P_j = P_{Nom} + \Delta P_{Off} + (\Delta P_G)_j + (\Delta P_R)_j \quad [25]$$

In order to calculate the disparity in distance between devices, we designate M1 as the point of reference, specifically as the transistor situated at the coordinates (0,0). It is possible to formulate a mathematical expression for the separation between transistors M1 and M_j in terms of D_{cc}. Additionally, the parameter Pj, which represents the degree of mismatch between these transistors, can be redefined as a function of P_Di_e. Notably, P_Di_e is a constant value that is specific to a given die, and is dependent on the distance between M1 and M_j. The objective of the present analysis is to acquire a deeper understanding of the impact of mismatch on the operational efficacy of a circuit, as implemented through a slice-based design methodology. Furthermore, the study aims to deliberate upon the preeminent mismatch parameters, namely β and Vt0.

2. Analysis and modelling of parameter scaling in semiconductor devices

The discourse delves into the ramifications of the parallel interconnection of transistors on the variability of specific electrical parameters within integrated circuits. The derivation of the equivalent mismatch parameter expression is contingent upon the quantity of transistors that are connected in parallel, which is represented as' k'.Afterscrutinizing the variance of the expression, it has been demonstrated to conform to Pelgrom's mismatch model, which adeptly accounts for the impact of both gradient and stochastic fluctuations.

Upon analysis, it has been determined that the utilization of slice-based analogue design technique is prone to variations related to gradient, particularly as the quantity of parallel-connected transistors is augmented. The observed phenomenon can be attributed to a discernible compromise between the operational efficacy of the device and the resultant vagaries stemming from mismatch effects, which are known to escalate with the value of k.

In order to evaluate the prevailing impact on a particular design, it is possible to compute a solitary k value that equates the variance of the two disparate mismatch effects. The determination of the value of k, symbolized as k*, necessitates the resolution of a polynomial expression. Conversely, when k exceeds k*, gradient distance-dependent variations demonstrate a higher degree of mismatch variance.

The passage elucidates the ramifications of parallel connection of transistors on the variability of specific electrical parameters in integrated circuits, and underscores the compromise between device efficacy and ambiguity resulting from mismatch effects. Furthermore, it proffers a technique for determining the ideal quantity of transistors connected in parallel that is best suited for a particular design.

E) Mismatch in Noise in Electronic Circuits

The thermal noise emanating from k transistors that are connected in parallel is contingent upon the quantity of transistors, k. The given expression encompasses a multitude of parameters, including but not limited to the modulation factor of channel length, transconductance, and overdrive of gate-source voltage. The significance of this data lies in its ability to elucidate the ramifications of transistor mismatch on circuit efficacy, thereby facilitating the refinement of circuitry for diminished noise.

F) Overview of Monte Carlo Simulations and Their Uses

A pair of MC simulations were executed to investigate the effects of mismatch on slices that are ctd in parallel. The initial simulation entailed a solitary transistor, with the aim of ascertaining the appropriateness of the proposed mismatch model in equation (25) for noise mismatch. The subsequent simulation was centered on the adaptable current sense amplifier (CSA) implemented in the integrated circuit (IC) design, with the aim of obtaining a deeper understanding of the circuit's performance under conditions of significant mismatch.

Each simulation was comprised of three distinct scenarios, namely those involving solely random variations, solely gradient variations, and a conflation of both effects. In order to optimize the lucidity of the graphed outcomes, the parameters of AVt0, Aβ, SVt0, and Sβ were subjectively chosen.

1. Overview of Monte Carlo Simulations and Their Uses

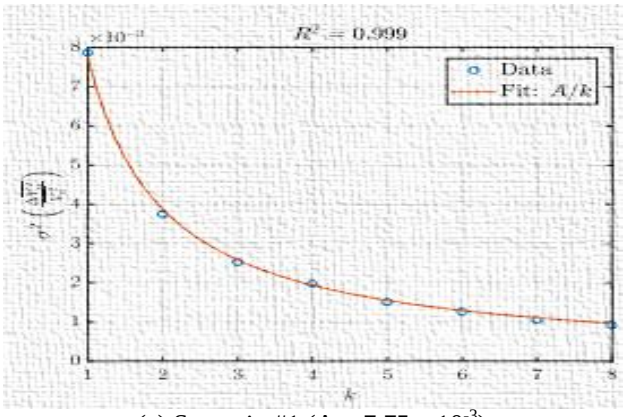
The outcomes of the MC simulations are depicted in Fig 22, accompanied by a scaled curve that is dependent on k. This scaling model was determined through the utilization of the nonlinear least-squares technique. The simulation findings suggest a close correlation between the noise mismatch and the proposed mismatch model (61) and (64), thereby establishing the validity and applicability of the model for a solitary equivalent transistor. The discovery implies that the proposed theoretical framework exhibits a high degree of precision in prognosticating the thermal noise of transistors that are interconnected in parallel. The simulations further elucidate the consequences of gradient mismatch on the circuit's noise, particularly when the quantity of parallel-connected slices is substantial. The outcomes furnish valuable discernments into the conduct of the circuit in instances where incongruity becomes pertinent, and have the potential to direct the formulation of noise-optimized integrated circuits [26].

2. Current-Steering Amplifier Simulation (CSA)

The behaviour of the o/p integrated noise of the CSA for each of the three simulation scenarios is shown in Figure 23. The

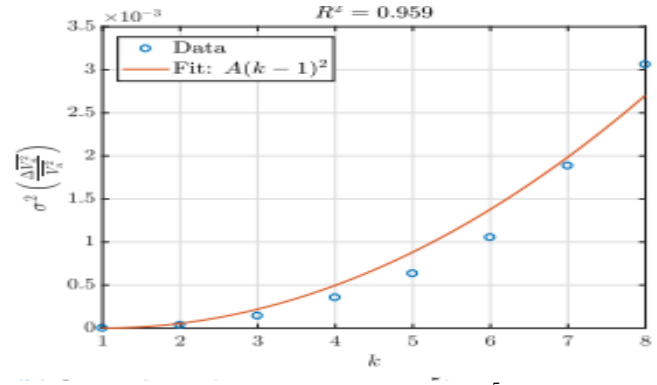
International Journal of Engineering Applied Sciences and Technology, 2024
Vol. 8, Issue 11, ISSN No. 2455-2143, Pages 98-113
Published Online March 2024 in IJEAST (http://www.ijeast.com)

proposed MSM (61) correctly predicts the behaviour of the o/p noise of the CSA, even though it was created from a single transistor, in scenario #1, where only size-dpd[t] mismatch is considered. This finding raises the possibility of constructing a generalized model, necessitating additional research.



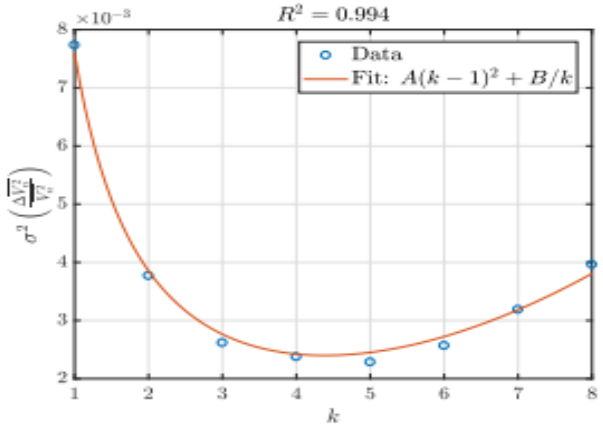
(a) Scenario #1 (A = 7.75 x 10^{-3})

Within the realm of statistical modelling of semiconductor device mismatches, the second scenario pertains solely to variations related to gradients. These variations arise from fluctuations in the doping concentration and oxide thickness within the active region of a MOSFET. In this scenario, it can be observed that the model expressed through equation (61) serves to partially anticipate the scaling tendencies of the gradient-associated discrepancy in relation to the scaling parameter k. Upon further examination of the findings, it has been determined that the gradient-associated inconsistency in relation to k does not precisely follow a quadratic pattern, and the model displays a tendency to underestimate the inconsistency for higher values of k. The root cause of this incongruity can be attributed to the allocation of noise variances, which do not conform to a normal distribution, but rather demonstrate a skewed distribution towards the right, as previously noted [14].



(b) Scenario #2 (A = 5.52 x 10^{-5})

In the third scenario, wherein a confluence of size and gradient-related discrepancies are considered, the model remains a sufficiently reliable prognosticator of the CSA's mismatch behaviour, albeit not infallible. In essence, the proposed model for mismatch scaling provides a foundation for evaluating the indeterminacy in the conduct of pertinent electrical characteristics resulting from mismatch.



(c) Scenario #2 (A = 5.83 x 10^{-5} , B = 7.59 x 10^{-3})

Fig 12. Analysis of Input-Referred Noise Variance in CSA Monte Carlo Simulation with Varying Number of Amplifier Slices and Simulation Scenarios

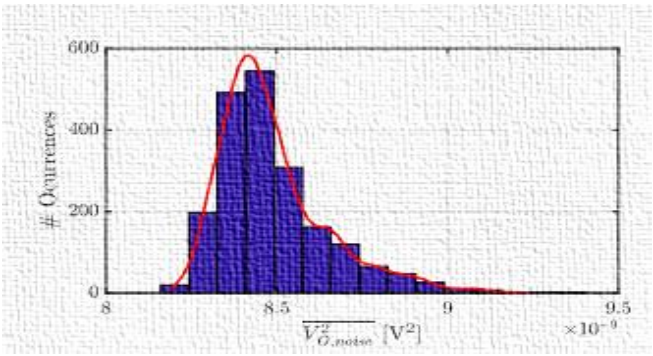


Fig 13. Analysis of Histogram of O/p Noise for k= '4' Considering Grad M/m[1]

VII. CONCLUSION

The present study introduces a novel methodology for the design of analogue integrated circuits, which is based on a slice-by-slice approach. The proposed methodology is intended for integration into EDA tools, with the objective of streamlining the user's workflow by minimizing the necessary time and level of expertise. The methodology is founded upon the utilization of preconceived and fine-tuned circuit modules, denoted as slices, which are exhaustively evaluated and can be linked in a parallel fashion to amplify critical performance parameters.The proposed methodology for design was subjected to validation via the configuration of a CSA that is adaptable, and the primary metric employed to assess the ckt was its noise performance. The empirical findings evince the

feasibility of mitigating circuit noise with ease and efficacy through the parallel interconnection of multiple amplifier slices, while exerting negligible influence on the amplifier's nominal operation [23].

Nonetheless, it is imperative to consider certain caveats that are specific to the problem at hand. Regarding the CSA, it is noteworthy that non-scaling cpct exert an impact on the amp b/width, which is observed to escalate with the addition of further slices that are cnctd in parallel. In the absence of bandwidth limitation for the amp, the augmentation of bandwidth would lead to a rise in the aggregate integrated noise on the output, thereby exerting an adverse impact on the primary performance parameter.

Moreover, the utilization of the stackable layout methodology in the design is notably vulnerable to device mismatch caused by gradients, which may become pertinent based on the cells pitch & quantity of parallel-ctd slices. The phenomenon of mismatch can give rise to a state of indeterminacy with regards to the anticipated operational efficacy of the circuit. The ambiguity may be accurately measured and evaluated through the implementation of suitable MSM and MC simulations. In its entirety, the slice-based design mthdlgy presents a promising avenue for analogue integrated circuit design, with the capacity to curtail design duration and enhance design efficacy [18].

The present study has put forth an e-URLLC framework that leverages edge computing to facilitate advancements in CE, thereby paving the way for "Consumer Electronics 2.0". The framework's inception was preceded by a compre^{v} review of the present state-of-the-art in CE. The proposed framework's pivotal facilitative techniques and instruments have undergone meticulous scrutiny. The explicit articulation of the "computing as a service" paradigm is anticipated to materialize through the advancement of 5G technologies. Furthermore, the Additionally Motivated device boasts a cost-effective and energy-efficient design that operates without a processor, possessing only minimal processing capabilities. It also features hybrid 5G capabilities. The exploration of potential inquiries and suggestions for the forthcoming generation of consumer electronics in the B5G/6G wireless era has been duly contemplated.

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